**Aim of the project:** The aim of the project is to design a 3-bit UWB Phase-shifter and implement one bit of it on a transmission line.

**Types of Phase Shifters:** The Phase shifters can be grouped in two types.

1. Ferrite Phase Shifters
2. PIN diode phase shifters

Ferrite Phase Shifters are activated by a pulsed current and power requirements are usually less than their PIN diode counterparts. Another issue that should be mentioned is that ferrite phase shifters are not reciprocal due to the characteristics of ferrite material. On the other hand, PIN diode phase shifters are smaller in size, integrable and have higher speed. Also circuitries implemented with PIN diodes occupy less area. However, diodes require continuous voltage and bias current which increases power consumption significantly. Basic types of PIN diode phase shifters are switched line, loaded line and reflection based phase shifters. In my project I had chosen to use switched line phase shifter due to the following advantages:

1. They can be easily cascaded in order to achieve higher amount of phase shift by controlling the increments of bias voltage. In my project, phase shifter is 3-bit and it can increase the phase shift at an amount between 0 or eight times of a unit shift amount (it is actually approximately 200ps in my project and eight bits cause 1.6ns delay at most).
2. They are used in broadband systems because distortion is minimized. I was expected to build a circuit which would operate over a wide range of frequency values.
3. They have a considerable power handling capacity.
4. They are inherently reciprocal.
5. Insertion loss is determined by the loss of the switches and line losses.

**Switched Line Phase Shifter:**

In this topology the amount of shifting is determined by the length of the transmission line. The losses in the line are due to the tangent loss of the FR4 and switching losses. As we know that although PIN diodes acts as short circuit when a certain potential difference between the nodes is exceeded, the amount of current is always limited to the amount of bias voltage. Thus there is always a resistance in the system in fact. But the resistance of the diode significantly reduces at higher voltage values. According to the measurements, the PIN diode available at our hand begins to conduct current of 0.5 mA when bias voltage exceeds 0.7 volts. After 1.2 volts amount of current is about 30 mA. We see that the resistance thus the loss of the switch reduces as voltage increases.

A schematic of 1-bit of the phase shifter is as follows:
The two branches of the phase shifter is set in such a way that never do both branches conduct the signal applied from the input port. The inductances are set at a high value because they are DC feed for the diodes and they actually do not allow the signal to reach to the ground. Series resistances are put to limit the amount of current drawn by diodes. Eventually they contribute to the impedance of the DC feed line and increasing it to a higher frequency and thus reducing the reflections. Another critical issue about the resistances is that when the current is limited the diodes have higher resistances, which in return increases the loss of the system and creates a mismatch of the impedance with respect to 50 Ohms and eventually increasing the reflections. However, because we do not know the actual characteristics of the diodes, The second effect will not be crucial in the simulations. But in order to obtain more realistic results and make them more approximate to real time measurements, I added some inductances and resistances on the lines.

In this configuration the upper branch determines the delay or phase shift amount. The diodes are used to set which path to conduct the incoming RF signal. In order to reduce the reflections in the upper branch, two diodes are used. The reason for this is if upper branch were not active when only one was used, that line would have a transmission line ended with open circuit. This would create the problem of distortion of the signal in the input node and increases the amount of the reflection from that port. To avoid such a problem additional diode must be used in expense of
additional loss and change (mismatch to 50 Ohms) in the input impedance of the overall system.

Input impedance of one stage phase shifter shows the following behaviour:

![Figure 2: Impedance vs. Frequency of 1-bit](image)

Overall input impedance can be observed as follows:

![Figure 3: Impedance vs. Frequency of 3-bit phase shifter](image)

The transmission lines in the system are consecutively 30mm, 60mm, 90mm. This gives us the opportunity to shift the signal upto 180mm electrical length.
Results of the simulations:

S parameters of the 3-bit phase shifter when 30mm and 90mm transmission lines are active are as follows.

<table>
<thead>
<tr>
<th>m1</th>
<th>freq=3.660GHz</th>
<th>m2</th>
<th>freq=10.00MHz</th>
<th>m3</th>
<th>freq=14.71GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>m1</td>
<td>=-0.547</td>
<td>m2</td>
<td>=31.389</td>
<td>m3</td>
<td>=20.040</td>
</tr>
</tbody>
</table>

![Figure 4: S parameters](image)

We can see that frequency goes up to 15 Ghz. But one thing that prevents the correct results are that the real parameters of the diodes are not entered to ADS when simulations are made.

![Figure 5: Transient response of the system](image)

As we can observe from the figure that pulse is shifted by an approximate amount of 800ps when 90mm and 30mm transmission lines are active. This can be calculated from the equation \( \Delta t \times v_p = L \), where \( v_p = 1.4e+8 \) m/s. And there is an insertion loss of 0.58 db which is quite good actually. The components used in the implementation are two DC blocking 0.1uF capacitors, two 7uH DC feed inductors, three high frequency PIN diodes. The resistors are not used because they cause significant reduction in the current passing through the diodes.
Measurements of the implemented circuit:

The characteristic of one-bit phase shifter can be deduced from the S parameters. Below the S-parameters (S11 and S21) of the system.

Figure 6: S21 at the OFF state
Figure 7: S11 at the OFF state

As we can observe from the two graphs, isolation and reflection are as they are expected to be at OFF state. No signal is transferred especially at lower frequencies, isolation provides the result up to 3.75 GHz. Second issue reflection are almost -1 dB up to 2 GHz. After 2.64 GHz the reflected signal drops to -3 dB which is the half power point.

When the bypass diode is opened, the following S11 and S21 graphs are obtained.

Figure 8: S11 when positive bias voltage is applied

Figure 9: S21 when positive bias voltage applied
When positive voltage is applied from the DC input, the diode in the lower branch of the schematic conducts current and thus becomes the path of the input signal. As we can see from the figures above @ 2.91 Ghz $S_{11}$ becomes -10dB. Until that point it seems to work with no problem. And also the highest amount of reflection up to 4.5 Ghz is the -6.6dB point @ 3.76 Ghz. $S_{21}$, transmission coefficient behaves similarly almost. At 2.79 Ghz, the signal is about -3dB half power point. So we can say that our circuit works up to 2.79 Ghz when positive bias voltage is applied.

$S_{21}$ and $S_{11}$ characteristics of the circuit when negative bias voltage is applied are as follows:

![Figure 10: $S_{11}$ when negative bias is applied](image)

The reflection coefficient is below -10dB up until 2.45 Ghz, which is not changed so much when compared to the previous one. There is -7.38 dB reflection at 2.66 Ghz but after that until 3 Gz it is again below -10 dB. If we assume that -7.4 dB can be an acceptable value, our characteristic is fine until 3.42 Ghz. As we see that there is a difference in $S_{11}$ of both conditions (negative bias and positive bias). The reason for this is that in the upper branch there stays two PIN diodes and transmission line is 6 cm which causes higher loss. So we can observe a reduction in the frequency range of circuit. Return loss for lower frequencies is high about on the order of 25 dB. Actually it is a good result.
The -3dB point is @ 2.4 GHz and until 4.43 GHz it is nearly -5.8 dB. We see that there is an insertion loss of -1db in the operating regime (62 Mhz-1.2Ghz). Then gradually it decreases. In general, we can observe that our circuit operates between 20 Mhz and 2.4 Ghz. Center frequency for this system is 1210 Mhz or 1.21 Ghz. Fractional bandwidth can be calculated as follows:

$$\text{FBW} = \frac{2.4 - 0.02}{2.4 + 0.02}$$

It has 95% fractional bandwidth which is quite reasonable.

After making S parameter calculations, digital anlayser infiniium oscilloscope is used to observe the transient response of the circuit. The chart below shows the details:

<table>
<thead>
<tr>
<th>Pulse_width</th>
<th>Bypass diode(+ bias)</th>
<th>Phase shifter mode(- bias)</th>
<th>OFF state(no bias)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.5 ns</td>
<td>Vo(-)/Vi(+)</td>
<td>.8015</td>
<td>.0465</td>
</tr>
<tr>
<td>1 ns</td>
<td>Vi(-)/Vi(+)</td>
<td>.7912</td>
<td>.0455</td>
</tr>
<tr>
<td>400 ps</td>
<td>Vo(-)/Vi(+)</td>
<td>.7764</td>
<td>.0667</td>
</tr>
<tr>
<td>100 ps</td>
<td>Vi(-)/Vi(+)</td>
<td>.7111</td>
<td>.0725</td>
</tr>
<tr>
<td>40 ps</td>
<td>Vo(-)/Vi(+)</td>
<td>.6011</td>
<td>.0911</td>
</tr>
</tbody>
</table>

TABLE 1: The measurements in the oscilloscope (sending a pulse)
In the OFF state, there is a considerable amount of reflection in the system which is about 0.4. However there is also some signal transferred to the output. The reason for this is the reverse bias and saturation Is current that flows through the junctions of the diode. This reduces the isolation of the phase shifter. Taking the logarithm of the value of the insertion, $-20\log(0.135)$, we obtain insertion loss as 17.39 dB which is fairly good actually. This provides us an isolation at OFF state. But in general operating conditions for example when there is a positive bias, insertion loss is $-20\log(0.71)=2.97$dB at 100ps pulse width. If we go further decreasing the pulse width to 40ps for instance, insertion loss becomes 4.43dB. Insertion loss at negative bias is worse than previous due to the fact that two series diodes reduce the power much more than one. For 400ps pulse width insertion loss is 2.2dB and for 100ps insertion loss is 4.4dB. In either case, return loss is quite high, about 22dB for 100ps pulse width.

The next observation for the phase shift is the amount of phase shift introduced by the 60mm transmission line for this. We can make the following observations from the oscilloscope.

*150ps pulse width:

In the first case we assume that there is no external bias (no positive or negative DC supply). Then this case is the OFF state for the phase shifter and it acts as a switch, isolating the output port from the input. For this case we had observed that S21 are quite well working upto 4.74 Ghz below -10dB. A significant amount of reflection is observed from Figure 12. But this is unavoidable because as we shut the diodes there remains no forward path for the signal to be transmitted. We can see that the amount of signal transmitted to the output is 0.04 Volt when 0.185 Volt is applied from the input. When the positive bias is applied, the reflection substatially decreases. The time domain analyses can be observed as follows:

![Figure 12: 150ps input signal OFF state](image1)

![Figure 13: 150ps input signal no_shift state](image2)

The transmitted signal is on the other hand is very low for OFF state but at a reasonable value when phase shifter is in no_shift state (positive bias). 0.025 Volt reflects back when 0.185 Volt is applied from the input. On the other hand when positive bias is applied on the by_pass diode
0.163V is transmitted to the output port. But the signal is widened a little bit due to not having so large bandwidth. For 150ps pulse not to be distorted, we need at least 6.6 Ghz bandwidth. Even though the results are not deviated from what we expected. The distortion is less. So we can count this working properly as a switch.

Figure14: 150ps OFF state output signal

Figure15: 150ps no_shift output signal

The last case is the case in which 60mm transmission line is the path that the signal is conducted. The figures 16 and 17 explains them in detail.

Figure16: 150ps input signal shifting mode

Figure17: 150ps output signal shifting mode

For this case we can easily observe that the amount of reflection from the input port has been increased. The reason for this is obvious due to the fact that two diodes causes more resistive losses rather than one. Two series resistance increase the impedance seen from port 1 and 2. Thus the reflection from both ports are higher when compared to by_pass diode is opened. It is about 0.03 Volt when the applied volatge is 185 mV. The amount of transmitted signal is about 0.145 V, which is actually quite adequate because 0.7838 of the signal is transmitted to the output and which means that it is operating above -3dB point. Comparing figures 15 and 17 we can find the amount of shift in the output signal. At no shift mode, the output signal is observed at 6.2 ns. Whereas at the shift
mode the output signal is at about 6.62ns. Taking these results into account, we can deduce the following result: The phase shifter has a 60 mm transmission line, which causes 420 ps time delay in the signal. But the total delay is not 420ps. The reason for this is there is still an inherent delay of the overall system, which is actually observed to be 150ps. This delay is eventually caused by the switching of the diodes. Thus at no shift mode, we are introduced 120ps time delay. At shifting mode this delay becomes about 150ps-200ps. Thus overall delay introduced by the system is about 600-620ps, 200ps of which is actually switching delay.

*500ps pulse width:

![Figure18: 500ps input OFF state](image1)

![Figure19: 500ps output OFF state](image2)

The results show us that when input signal of 0.185 V is sent, 0.09 V reflection occurs and 0.025 V is transmitted to the output. The insertion loss is about 17.38 dB which is quite good.

![Figure20: 500ps input no_shift mode](image3)

![Figure21: 500ps output no_shift mode](image4)

We can see that RL is quite high for this case as we have been expected. The transmitted voltage is about 0.15 V where the input signal is 0.185 V. 0.81 of the input voltage is transmitted to the output port.
From the figures above we see that RL is still quite high. 0.147 V of 0.185 V has been transmitted to the output port. Actually IL from this ratio can be found as 2dB, which is in fact quite good. When we compare the figures 21 and 23, we will find out amount of phase shift with respect to the outputs. From the figure it can be observed that 410ps has been introduced. However, the overall delay for the shifting case is 600 ps and for the no shifting case is 190ps. For wider pulses the insertion loss does not change so much, it is typically between 1.5dB and 2.5 dB between 5ns pulse and 200ps pulse. After 200ps going towards smaller pulse width, it begins to drop significantly and at 100ps it is about -3dB.

Conclusions:

Simulation and implementation differ great due to the fact that losses and extra parasitics are inherently available in the circuit and reduce the performance of the circuit. Also FR4 board can operate upto 8-10 Ghz. It has finite tangent loss. Connections between components produce parasitics inductances, which actually degrade the performance of the circuit. So in the simulation, we should carefully add all these parasitic effects, losses and accurate component models to obtain better and accurate results. However the amount of phase shift that we introduced to the does not change and it is nearly 410ps as we had previously calculated. The IL and RL are quite good actually. However, there is still a bandwidth problem. In the semester, I will deal with the improvement of this circuitry.